

DATA SHEET

SAA5700

Chinese Character System Teletext (CCST) decoder

Preliminary specification
File under Integrated Circuits, IC02

1997 May 16

Chinese Character System Teletext (CCST) decoder

SAA5700

FEATURES

- Acquisition and display of the 625-line PAL CCST Chinese standard for teletext, with Chinese and Latin character sets
- Supports multiple DRAM sizes: 256K × 4 bits, 1M × 4 bits, 4M × 4 bits and 2 × 1M × 4 bits with an additional decoder/demultiplexer IC
- Acquires and stores in background up to (typically) 400 pages with 1M × 4 bits external DRAM
- CCST Fastext, with capability of displaying Chinese characters on Fastext prompt row
- Meshing for reduced contrast video background in subtitles and boxes
- Full line and screen colour to all edges of screen
- Supports 625-line 50/100 Hz display modes
- Scan-locked and stand-alone sync modes; supports video-locked sync modes with external PLL
- Easy control via high level I²C-bus SAFARI commands
- Sync mode switching and picture centring via I²C-bus SAFARI commands
- Supports external decryption unit for encrypted data.



GENERAL DESCRIPTION

The SAA5700 is a Chinese teletext decoder suitable for TV and multimedia applications. It incorporates all the data slicing, acquisition and display circuitry on-chip, as well as the logic for memory management. An external DRAM is used to store the currently displayed page and also the precaptured teletext pages.

An external ROM is used to store the ideographic Chinese character set. There is a high level software interface with easy commands for the control of the decoder. Control is achieved via the I²C-bus.

The device is available in a QFP64 package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5700GP	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

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BLOCK DIAGRAM

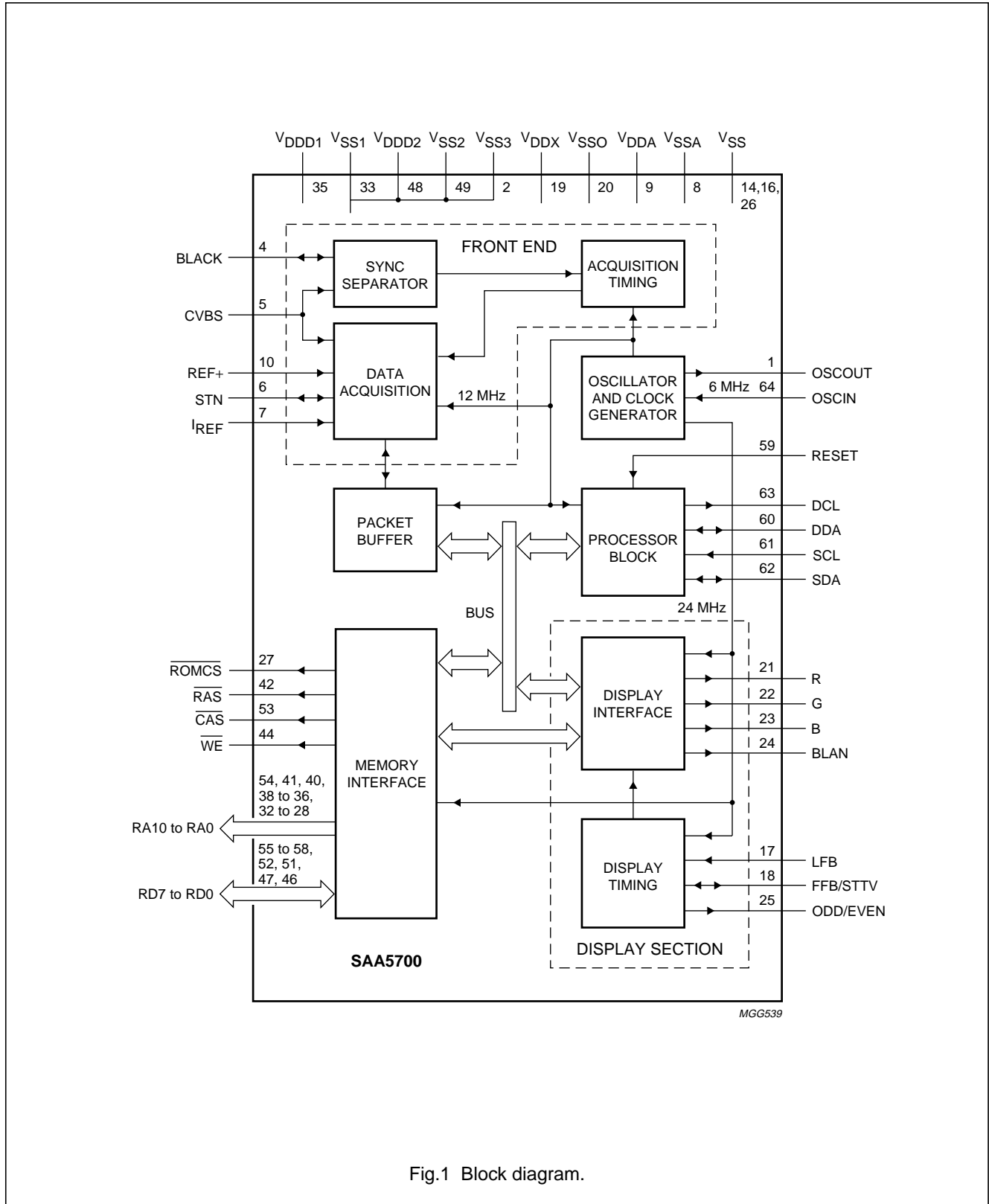


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	I/O	DESCRIPTION
OSCOUT	1	O	oscillator output to crystal
V _{SS3}	2	ground	ground for I/O pad buffers connect to V _{SS} ; internally connected to V _{SS1} and V _{SS2}
n.c.	3	–	not connected
BLACK	4	I/O	black level sample and hold capacitor; 100 nF to V _{SSA}
CVBS	5	I	video signal input; 100 nF series capacitor, 250 Ω source impedance maximum, reference to V _{SSA}
STN	6	I/O	ADC current reference decoupling; 100 nF to V _{SSA}
I _{REF}	7	I	current reference input; 10 kΩ to V _{SSA}
V _{SSA}	8	ground	0 V power supply; analog
V _{DDA}	9	supply	+5 V power supply; analog
REF+	10	I	ADC voltage reference decoupling; 100 nF to V _{SSA}
i.c.	11	–	internally connected; do not use
i.c.	12	–	internally connected; do not use
i.c.	13	–	internally connected; do not use
V _{SS}	14	ground	connect to V _{SS} for normal use
n.c.	15	–	not connected
V _{SS}	16	ground	connect to V _{SS} for normal use
LFB	17	I	scan line flyback input (HSYNC)
FFB/STTV	18	I/O	scan field flyback input (VSYNC)/sync to TV output
V _{DDX}	19	supply	+5 V power supply; connect to V _{DD} for normal use
V _{SSO}	20	ground	output stage current return and 0 V
R	21	O	analog Red output
G	22	O	analog Green output
B	23	O	analog Blue output
BLAN	24	O	fast blanking (VDS)
ODD/EVEN	25	O	frame rate signal for hardware de-interlace (FRAME)
V _{SS}	26	ground	connect to V _{SS} for normal use
ROMCS	27	O	chip select (address decode) for ROM
RA0	28	O	bit 0 of address to DRAM, ROM and IC
RA1	29	O	bit 1 of address to DRAM, ROM and IC
RA2	30	O	bit 2 of address to DRAM, ROM and IC
RA3	31	O	bit 3 of address to DRAM, ROM and IC

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SYMBOL	PIN	I/O	DESCRIPTION
RA4	32	O	bit 4 of address to DRAM, ROM and IC
V _{SS1}	33	ground	0 V power supply digital; connected internally to V _{SS2} and V _{SS3}
n.c.	34	–	not connected
V _{DD1}	35	supply	+5 V power supply digital; connected internally to V _{DD2}
RA5	36	O	bit 5 of address to DRAM, ROM and IC
RA6	37	O	bit 6 of address to DRAM, ROM and IC
RA7	38	O	bit 7 of address to DRAM, ROM and IC
n.c.	39	–	not connected
RA8	40	O	bit 8 of address to DRAM, ROM and IC
RA9	41	O	bit 9 of address to DRAM, ROM and IC
$\overline{\text{RAS}}$	42	O	row address strobe to DRAM; active LOW
n.c.	43	–	not connected
$\overline{\text{WE}}$	44	O	write enable to DRAM and IC; active LOW
i.c.	45	–	internally connected; do not use
RD0	46	I/O	bit 0 of data bus to/from DRAM, ROM and IC
RD1	47	I/O	bit 1 of data bus to/from DRAM, ROM and IC
V _{DD2}	48	supply	+5 V power supply digital; connected internally to V _{DD1}
V _{SS2}	49	ground	0 V power supply digital; connected internally to V _{SS1} and V _{SS3}
n.c.	50	–	not connected
RD2	51	I/O	bit 2 of data bus to/from DRAM, ROM and IC
RD3	52	I/O	bit 3 of data bus to/from DRAM, ROM and IC
$\overline{\text{CAS}}$	53	O	column address strobe to DRAM; active LOW
RA10	54	O	bit 10 of address to DRAM, ROM and IC
RD7	55	I/O	bit 7 of data bus to/from DRAM, ROM and IC
RD6	56	I/O	bit 6 of data bus to/from DRAM, ROM and IC
RD5	57	I/O	bit 5 of data bus to/from DRAM, ROM and IC
RD4	58	I/O	bit 4 of data bus to/from DRAM, ROM and IC
RESET	59	I	chip/processor reset input (active HIGH)
DDA	60	I/O	bidirectional serial data to/from optional Decryptor
SCL	61	I	primary I ² C-bus serial clock input
SDA	62	I/O	primary I ² C-bus serial data
DCL	63	O	serial clock to optional Decryptor
OSCIN	64	I	oscillator input from crystal/external clock input

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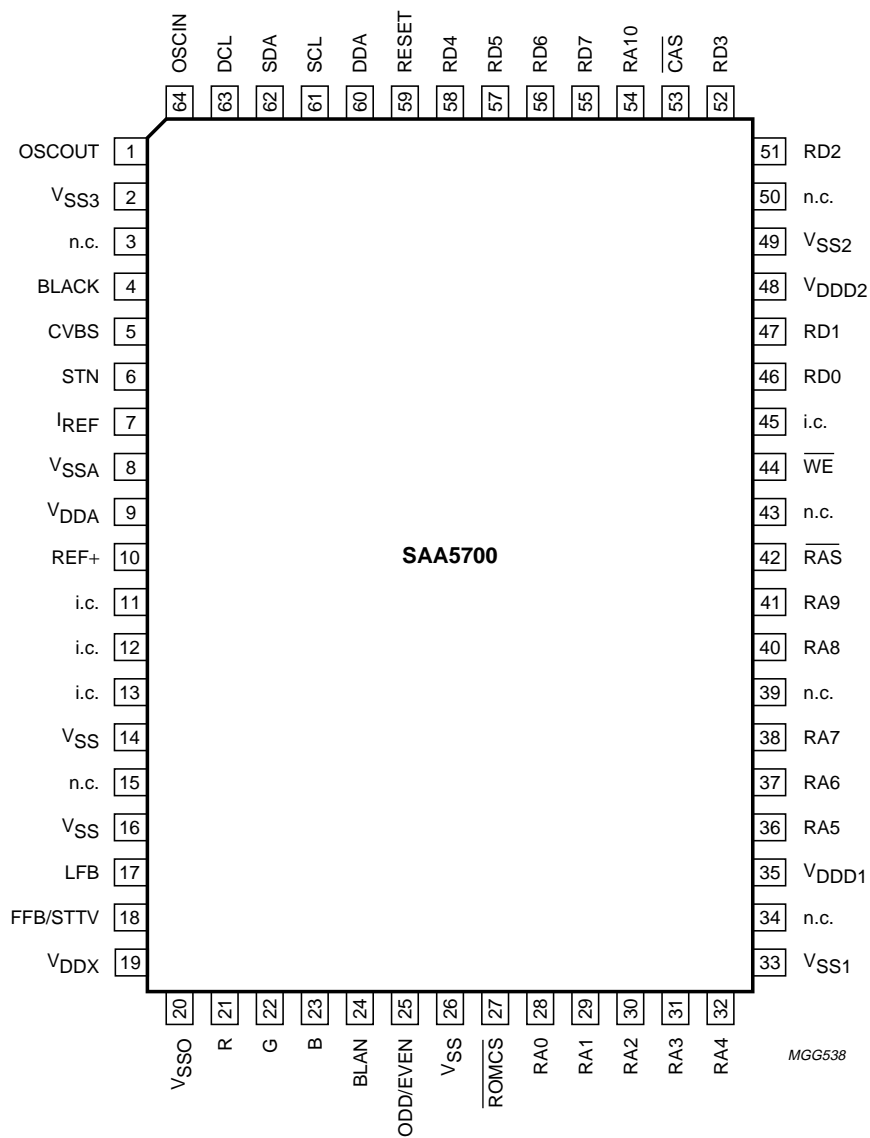


Fig.2 Pin configuration.

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HIGH LEVEL I²C-BUS COMMAND INTERFACE

This device communicates via the I²C-bus using the SAFARI protocol. The following section indicates the protocol which is supported by this decoder.

User commands

Table 1 lists the CCST user command codes in TV mode; Table 2 lists the CCST user command codes in Text mode.

Table 1 TV mode user command codes

FUNCTION ID (HEX)	FUNCTION
00	–
01	–
02	–
03	PICTURE
04	STATUS
05	–
06	–
07	TIME
08	–
09	–
0A	–
0B	–
0C	–
0D	–
0E	–
0F	–
10	TV PROGRAMME 0
11	TV PROGRAMME 1
12	TV PROGRAMME 2
13	TV PROGRAMME 3
14	TV PROGRAMME 4
15	TV PROGRAMME 5
16	TV PROGRAMME 6
17	TV PROGRAMME 7
18	TV PROGRAMME 8
19	TV PROGRAMME 9
1A	TV PROGRAMME 10
1B	TV PROGRAMME 11
1C	TV PROGRAMME 12
1D	TV PROGRAMME 13
1E	TV PROGRAMME 14
1F	TV PROGRAMME 15

Table 2 Text mode user command codes

FUNCTION ID (HEX)	FUNCTION
20	RED
21	GREEN
22	YELLOW
23	SUBTITLE
24	STATUS
25	HOLD TOGGLE
26	REVEAL
27	CANCEL TOGGLE
28	INDEX
29	–
2A	BROWSE
2B	REVEAL SET TOGGLE
2C	–
2D	PREVIOUS
2E	DISPLAY CHINESE PROMPT
2F	SUBCODE TOGGLE
30	1
31	2
32	3
33	4
34	5
35	6
36	7
27	8
28	9
29	0
3A	SIZE
3B	UP
3C	DOWN
3D	CYAN
3E	MIX
3F	TEXT

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Extended commands

The extended commands for the decoder are listed in Table 3.

Table 3 Extended commands

OBJECT		FUNCTION		PARAMETER LENGTH (BYTES)		PARAMETERS	
NAME	ID (HEX)	NAME	ID (HEX)	INPUT	OUTPUT	INPUT	OUTPUT
Display	48	set sync mode	04	1	–	sync mode	none
		set display position	08	4	–	row start, line start	none
Processor	52	restart software	06	3	–	FFFFFFCH	none
Memory and OSD	53	read packet	03	1 [+1]	40	packet number, [Designation code]	packet data
		write packet	06	1 +40	–	packet number, packet data	none
		OSD mode on	08	0	–	none	none
		OSD mode off	0A	0	–	none	none
		OSD display	0E	0	–	none	none
		clear display page	10	0	–	none	none

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
V _{DDD1}	digital supply voltage 1	-0.3	+6.5	V
V _{DDD2}	digital supply voltage 2	-0.3	+6.5	V
V _{DDA}	analog supply voltage	-0.3	+6.5	V
V _{DDX}	supply voltage X	-0.3	+6.5	V
V _{I(max)}	maximum input voltage (any input)	-0.3	V _{DD} + 0.5	V
V _{O(max)}	maximum output voltage (any output)	-0.3	V _{DD} + 0.5	V
ΔV _{DDX-DDn}	supply voltage difference between V _{DDX} , V _{DDD1} , V _{DDD2} and V _{DDA}	-	0.25	V
I _{I(d)}	diode input current (DC)	-	20	mA
I _{O(d)}	diode output current (DC)	-	20	mA
I _{O(max)}	maximum output current (any output)	-	10	mA
T _{stg}	storage temperature	-55	+125	°C
T _{amb}	operating ambient temperature	-20	+70	°C

CHARACTERISTICS

T_{amb} = -20 to +70 °C and V_{DDn} = 4.5 to 5.5 V; unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supplies						
V _{DDD1}	digital supply voltage 1		4.5	5.0	5.5	V
I _{DDD1}	digital supply current 1		-	95	140	mA
V _{DDD2}	digital supply voltage 2		4.5	5.0	5.5	V
I _{DDD2}	digital supply current 2		-	2.4	6.5	mA
V _{DDA}	analog supply voltage		4.5	5.0	5.5	V
I _{DDA}	analog supply current		-	40	53	mA
V _{DDX}	supply voltage X		4.5	5.0	5.5	V
I _{DDX}	supply current X		-	32	40	mA
I _{DD(tot)}	total supply current		-	170	240	mA
Inputs						
CVBS						
V _{sync}	sync amplitude		0.1	0.3	0.6	V
V _{bur(p-p)}	colour burst amplitude (peak-to-peak value)		0	0.3	4	V
V _{I(video)(p-p)}	video input amplitude (peak-to-peak value)		0.7	1.0	1.4	V
V _{I(data)}	teletext data amplitude		0.29	0.46	0.71	V
Z _{source}	source impedance		-	-	250	Ω
V _{SW(l)}	input switching level of sync separator		1.6	1.9	2.2	V
C _i	input capacitance		-	-	10	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{REF}						
R _{IREF}	resistor to V _{SSA}		–	10	–	kΩ
V _{IREF}	voltage on I _{REF} pin	V _{DD} = 5 V	–	2.3	–	V
RESET						
V _{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V _{IH}	HIGH-level input voltage		2.0	–	V _{DD} + 0.5	V
I _{LI}	input leakage current	V _I = 0 to V _{DD}	–10	–	+10	μA
LFB (HSYNC)						
V _{IL}	LOW-level input voltage		–0.3	–	+0.6	V
V _{IH}	HIGH-level input voltage		2.4	–	V _{DD} + 0.5	V
V _{hys}	input hysteresis voltage		–	0.7	–	V
I _{LI}	input leakage current	V _I = 0 to V _{DD}	–10	–	+10	mA
I _{I(max)}	maximum input current	note 1	–1	–	+1	μA
t _{W(LFB)}	LFB input pulse width		200	–	–	ns
t _{i(r)}	input rise time		–	–	100	ns
t _{i(f)}	input fall time		–	–	100	ns
FFB (VSYNC)						
V _{IL}	LOW-level input voltage		–0.3	0.3V _{DD}	–	V
V _{IH}	HIGH-level input voltage		0.7V _{DD}	V _{DD} + 0.5	–	V
I _{LI}	input leakage current	V _I = 0 to V _{DD}	–10	+10	–	μA
I _{I(max)}	maximum input current		–1	+1	–	mA
t _{W(FFB)}	FFB input pulse width		1	–	–	display lines
t _{i(r)}	input rise time		–	–	500	ns
t _{i(f)}	input fall time		–	–	500	ns
Input/outputs						
REF+						
C _{REF+}	decoupling capacitor to V _{SSA}		–	100	–	nF
V _{REF+}	DC voltage on REF+		2.3	2.5	2.7	V
OSCIN AND OSCOUT						
V _{osc(p-p)}	oscillation amplitude (peak-to-peak value)		–	V _{DD}	–	V
C _i	input capacitance		–	–	10	pF
f _{osc}	oscillator frequency		–	6.0	–	MHz
Δf _{osc}	oscillator frequency tolerance		–	500	–	ppm
BLACK						
C _{BLACK}	storage capacitor to V _{SSA}		–	100	–	nF
V _{BLACK}	black level for nominal sync amplitude		1.75	2.0	2.25	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	input leakage current	$V_I = 0$ to V_{DD}	-10	-	+10	μA
STN						
C_{STN}	decoupling capacitor to V_{SSA}		-	100	-	nF
V_{STN}	DC voltage on STN		0.95	1.1	1.25	V
SCL (OPEN-DRAIN)						
f_{SCL}	SCL clock frequency		0	-	400	kHz
V_{IL}	LOW-level input voltage		-0.5	-	+1.5	V
V_{IH}	HIGH-level input voltage		3.0	-	$V_{DD} + 0.5$	V
V_{OL}	LOW-level output voltage	$I_{OL} = 3$ mA	0	-	0.4	V
		$I_{OL} = 6$ mA	0	-	0.6	V
I_{LI}	input leakage current	$V_I = 0$ to V_{DD}	-10	-	+10	μA
C_i	input capacitance		-	-	10	pF
C_L	load capacitance		-	-	400	pF
$t_{i(r)}$	input rise time	$f_{SCL} = 100$ kHz; note 2	50	-	1000	ns
		$f_{SCL} = 400$ kHz; note 2	50	-	300	ns
$t_{i(f)}$	input fall time	$f_{SCL} = 100$ kHz; note 3	50	-	300	ns
		$f_{SCL} = 400$ kHz; note 3	50	-	300	ns
$t_{o(f)}$	output fall time	3 to 1.5 V; $I_{OL} = 3$ mA	50	-	250	ns
SDA (OPEN-DRAIN)						
V_{IL}	LOW-level input voltage		-0.5	-	+1.5	V
V_{IH}	HIGH-level input voltage		3.0	-	$V_{DD} + 0.5$	V
V_{OL}	LOW-level output voltage	$I_{OL} = 3$ mA	0	-	0.4	V
		$I_{OL} = 6$ mA	0	-	0.6	V
I_{LI}	input leakage current	$V_I = 0$ to V_{DD}	-10	-	+10	μA
C_i	input capacitance		-	-	10	pF
C_L	load capacitance		-	-	400	pF
$t_{i(r)}$	input rise time	$f_{SCL} = 100$ kHz; note 2	50	-	1000	ns
		$f_{SCL} = 400$ kHz; note 2	50	-	300	ns
$t_{i(f)}$	input fall time	$f_{SCL} = 100$ kHz; note 3	50	-	300	ns
		$f_{SCL} = 400$ kHz; note 3	50	-	300	ns
$t_{o(f)}$	output fall time	3 to 1.5 V; $I_{OL} = 3$ mA	50	-	250	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCL AND DDA (INTERNAL PULL-DOWN RESISTOR)						
V _{IL}	LOW-level input voltage		-0.3	-	+0.8	V
V _{IH}	HIGH-level input voltage		2.0	-	V _{DD} + 0.5	V
V _{OL}	LOW-level output voltage	I _{OL} = 1.6 mA	0	-	0.4	V
I _{LI}	input leakage current	V _I = 0 to V _{DD}	-10	-	+10	μA
C _i	input capacitance		-	-	10	pF
C _L	load capacitance		-	-	50	pF
t _{o(f)}	output fall time	2.2 to 0.6 V; I _{OL} = 1.6 mA	-	-	10	ns
RD7 TO RD0						
V _{IL}	LOW-level input voltage		-0.3	-	+0.8	V
V _{IH}	HIGH-level input voltage		2.0	-	V _{DD} + 0.5	V
V _{OL}	LOW-level output voltage	I _{OL} = 1.6 mA	0	-	0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = -0.2 mA	2.4	-	V _{DD}	V
I _{LI}	input leakage current	V _I = 0 to V _{DD}	-10	-	+10	μA
C _i	input capacitance		-	-	10	pF
C _L	load capacitance		-	-	30	pF
t _{o(r)}	output rise time into C _L	0.6 to 2.2 V	-	-	10	ns
t _{o(f)}	output fall time into C _L	2.2 to 0.6 V	-	-	10	ns
Outputs						
CAS						
V _{OL}	LOW-level output voltage	I _{OL} = 1.6 mA	0	-	0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = -0.2 mA	2.4	-	V _{DD}	V
C _L	load capacitance		-	-	50	pF
t _{o(r)}	output rise time into C _L	0.6 to 2.2 V	-	-	5	ns
t _{o(f)}	output fall time into C _L	2.2 to 0.6 V	-	-	5	ns
RAS, WE, ROMCS, RA10 TO RA0						
V _{OL}	LOW-level output voltage	I _{OL} = 1.6 mA	0	-	0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = -0.2 mA	2.4	-	V _{DD}	V
C _L	load capacitance		-	-	50	pF
t _{o(r)}	output rise time into C _L	0.6 to 2.2 V	-	-	10	ns
t _{o(f)}	output fall time into C _L	2.2 to 0.6 V	-	-	10	ns
ODD/EVEN (FRAME)						
V _{OL}	LOW-level output voltage	I _{OL} = 1.6 mA	0	-	0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = -0.2 mA	2.4	-	V _{DD}	V
C _L	load capacitance		-	-	200	pF
t _{o(r)}	output rise time into C _L	0.6 to 2.2 V	-	-	200	ns
t _{o(f)}	output fall time into C _L	2.2 to 0.6 V	-	-	200	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
STTV						
V_{STTV}	VCS, TCS amplitude		0.2	0.3	0.4	V
$V_{STTV(DC)}$	nominal DC voltage		1.85	2.0	2.15	V
$I_{O(drive)}$	output drive		–	–	3	mA
R, G AND B						
I_{OL}	LOW-level output current (black level)		–10	–	+10	μ A
I_{OH}	HIGH-level output current (full intensity)	$V_{DDX} = 5\text{ V}$	5.1	6.0	6.9	mA
R_L	load resistance to V_{SSO} for nominal 1 V _(p-p) output		–	160	–	Ω
C_L	load capacitance		–	–	20	pF
$t_{o(r)}$	output rise time	10% to 90%	–	–	15	ns
$t_{o(f)}$	output fall time	90% to 10%	–	–	15	ns
BLAN (VDS)						
V_{OH}	HIGH-level output voltage	$I_{OH} = -2\text{ mA}$	$V_{DD} - 0.25$	–	V_{DD}	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2\text{ mA}$	0	–	0.2	V
C_L	load capacitance		–	–	50	pF
$t_{o(r)}$	output rise time	10% to 90%	–	–	15	ns
$t_{o(f)}$	output fall time	90% to 10%	–	–	15	ns
t_{SK}	skew delay between outputs R,G,B and BLAN		–	–	15	ns

Notes

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. An external series resistor must be used to limit the input currents to 1 mA.
2. Measured from $V_{IL(max)}$ to $V_{IH(min)}$.
3. Measured from $V_{IH(min)}$ to $V_{IL(max)}$.

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Table 4 I²C-bus Timing (see note 1 and Fig.3)

SYMBOL	PARAMETER	100 kHz		400 kHz		UNIT
		MIN.	MAX.	MIN.	MAX.	
f _{SCL}	SCL clock frequency	0	100	0	400	kHz
t _{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	μs
t _{HIGH}	HIGH period of the SCL clock	4.0	–	0.6	–	μs
t _{SU;DAT}	data set-up time	250	–	100	–	μs
t _{HD;DAT}	date hold time	0	–	0	–	μs
t _{SU;STO}	set-up time clock HIGH to STOP	4.7	–	0.6	–	μs
t _{BUF}	set-up time STOP to START	4.7	–	1.3	–	μs
t _{HD;STA}	START hold time	4.0	–	0.6	–	μs
t _{SU;STA}	set-up time clock rising edge to START	4.7	–	0.6	–	μs
t _r	rise time of both SDA and SCL signals	–	1000	–	300	ns
t _f	fall time of both SDA and SCL signals	–	300	–	300	ns

Note

1. The I²C-bus interface pins SDA and SCL may pull the data and clock lines below 3 V while the power supply V_{DD} is in the range 0.4 to 0.8 V. Outside this range, the SDA and SCL pins behave correctly.

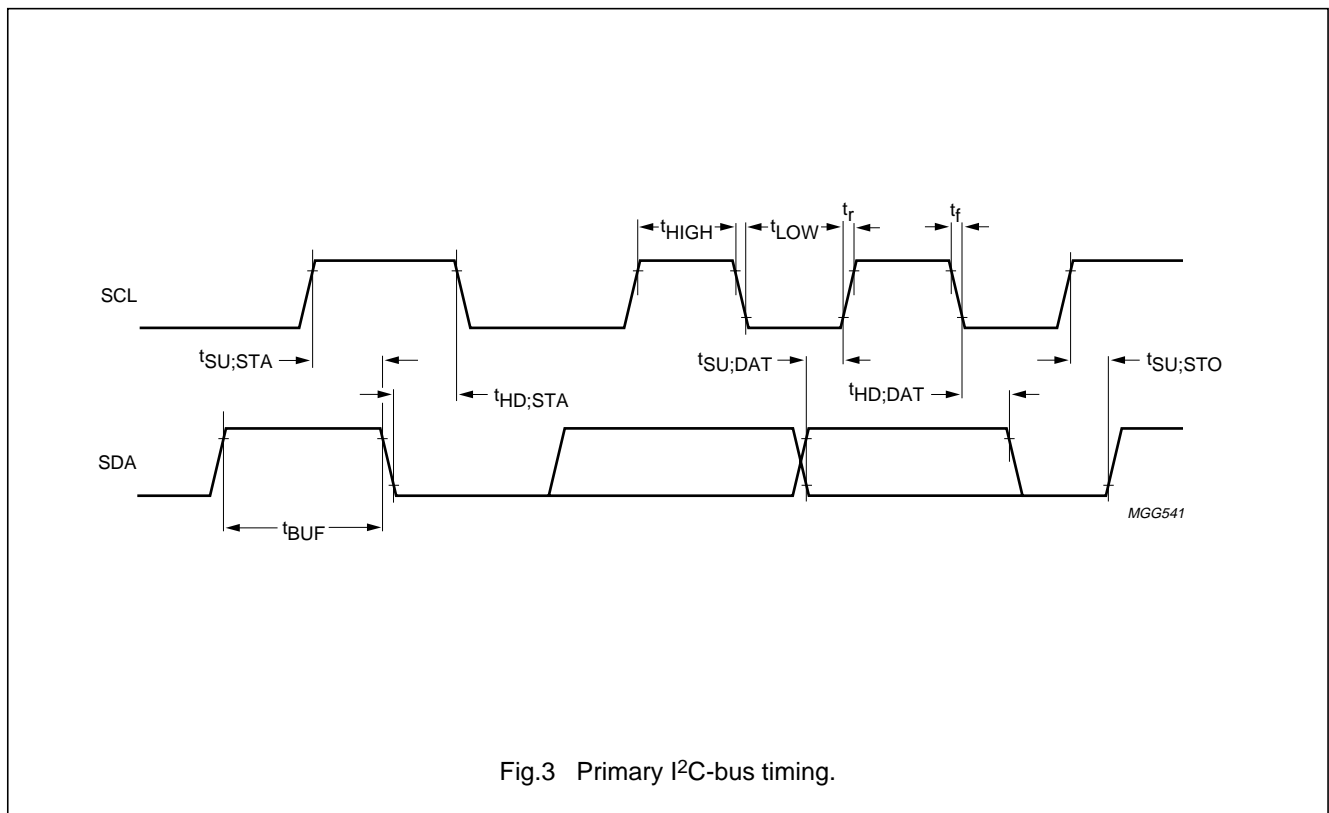


Fig.3 Primary I²C-bus timing.

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DRAM Interface timing (see note 1 and Fig.4)

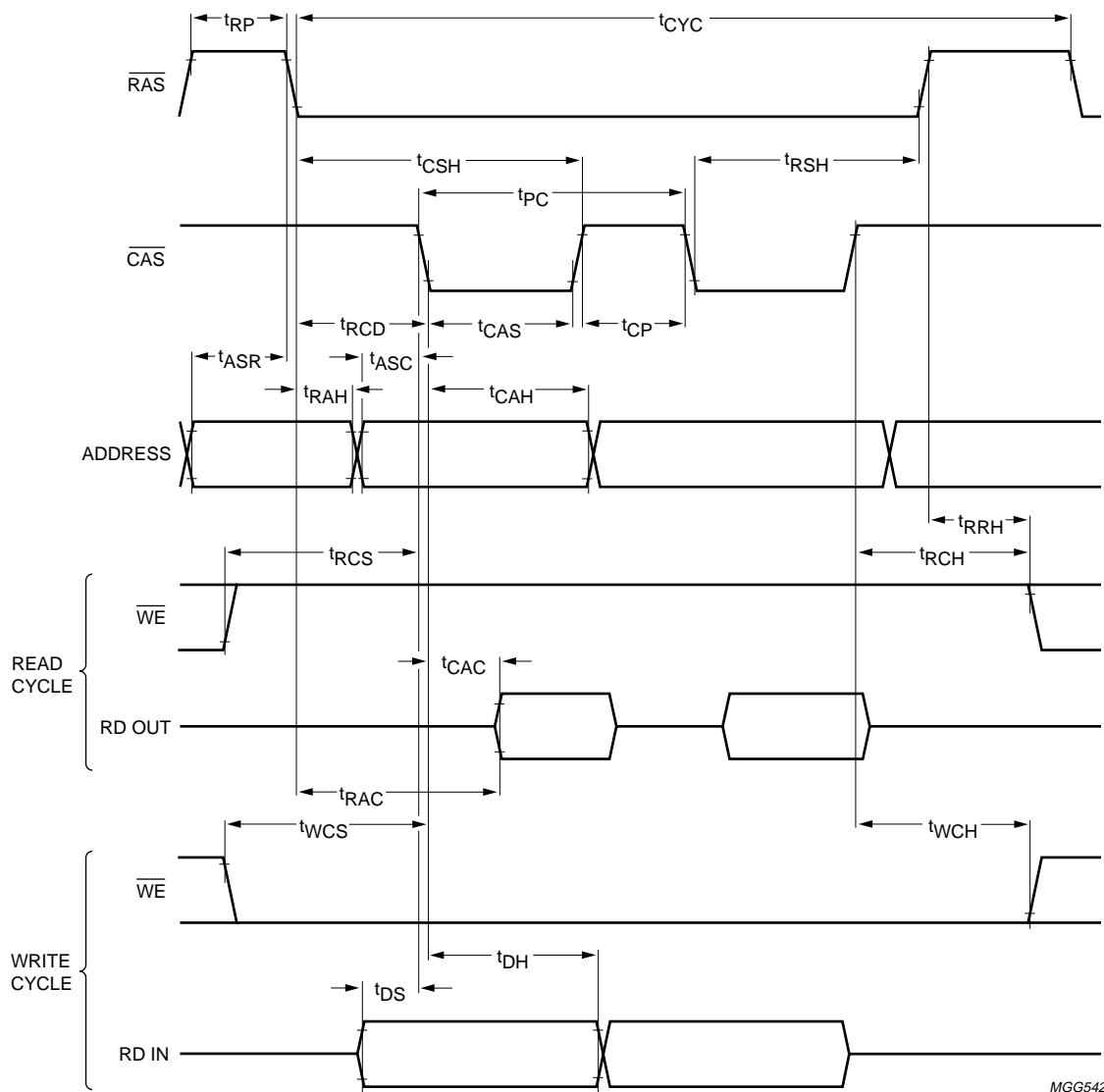
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$T_{cy}(RAS)$	\overline{RAS} cycle time	–	375	–	ns
$t_{pch}(RAS)$	\overline{RAS} precharge time	60	–	–	ns
$t_h(CAS)$	\overline{CAS} hold time	80	–	–	ns
$t_d(RAS-CAS)$	\overline{RAS} to \overline{CAS} delay time	20	–	–	ns
$t_{WL}(CAS)$	\overline{CAS} pulse width LOW	20	–	–	ns
$T_{cy}(CAS)$	\overline{CAS} page mode cycle time	50	–	–	ns
$t_{pch}(CAS)$	\overline{CAS} precharge time	10	–	–	ns
$t_h(CAS-RAS)$	\overline{RAS} hold time after \overline{CAS}	20	–	–	ns
$t_{pch}(CAS-RAS)$	\overline{CAS} to \overline{RAS} precharge time	10	–	–	ns
$t_{su}(RA)$	row address set-up time	0	–	–	ns
$t_h(RA)$	row address hold time	10	–	–	ns
$t_{su}(CA)$	column address set-up time	0	–	–	ns
$t_h(CA)$	column address hold time	15	–	–	ns
$t_{su}(R)$	read command set-up time	0	–	–	ns
$t_h(R)(CAS)$	read command hold time from (\overline{CAS})	0	–	–	ns
$t_h(R)(RAS)$	read command hold time from (\overline{RAS})	10	–	–	ns
$t_{su}(W)$	write command set-up time	0	–	–	ns
$t_h(W)$	write command hold time	15	–	–	ns
$t_{su}(i)(D)$	data input set-up time	0	–	–	ns
$t_h(i)(D)$	data input hold time	15	–	–	ns
$t_{ACC}(R)(CAS)$	read access time from (\overline{CAS})	–	–	20	ns
$t_{ACC}(R)(RAS)$	read access time from (\overline{RAS})	–	–	80	ns

Note

1. Based on a display clock frequency of 24 MHz, maximum 24 MHz + 500 ppm.

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MGG542

Fig.4 DRAM interface timing.

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APPLICATION INFORMATION

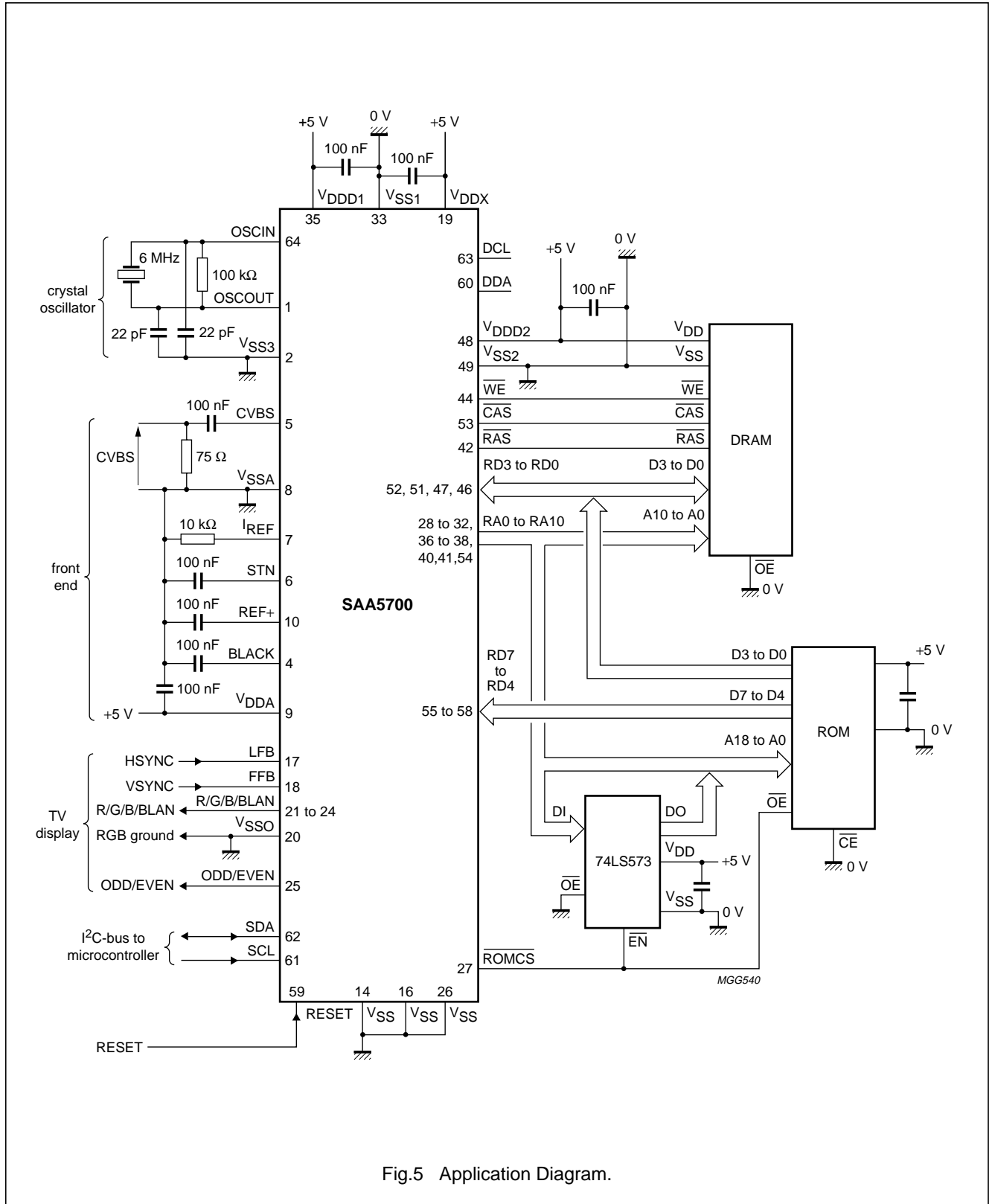


Fig.5 Application Diagram.

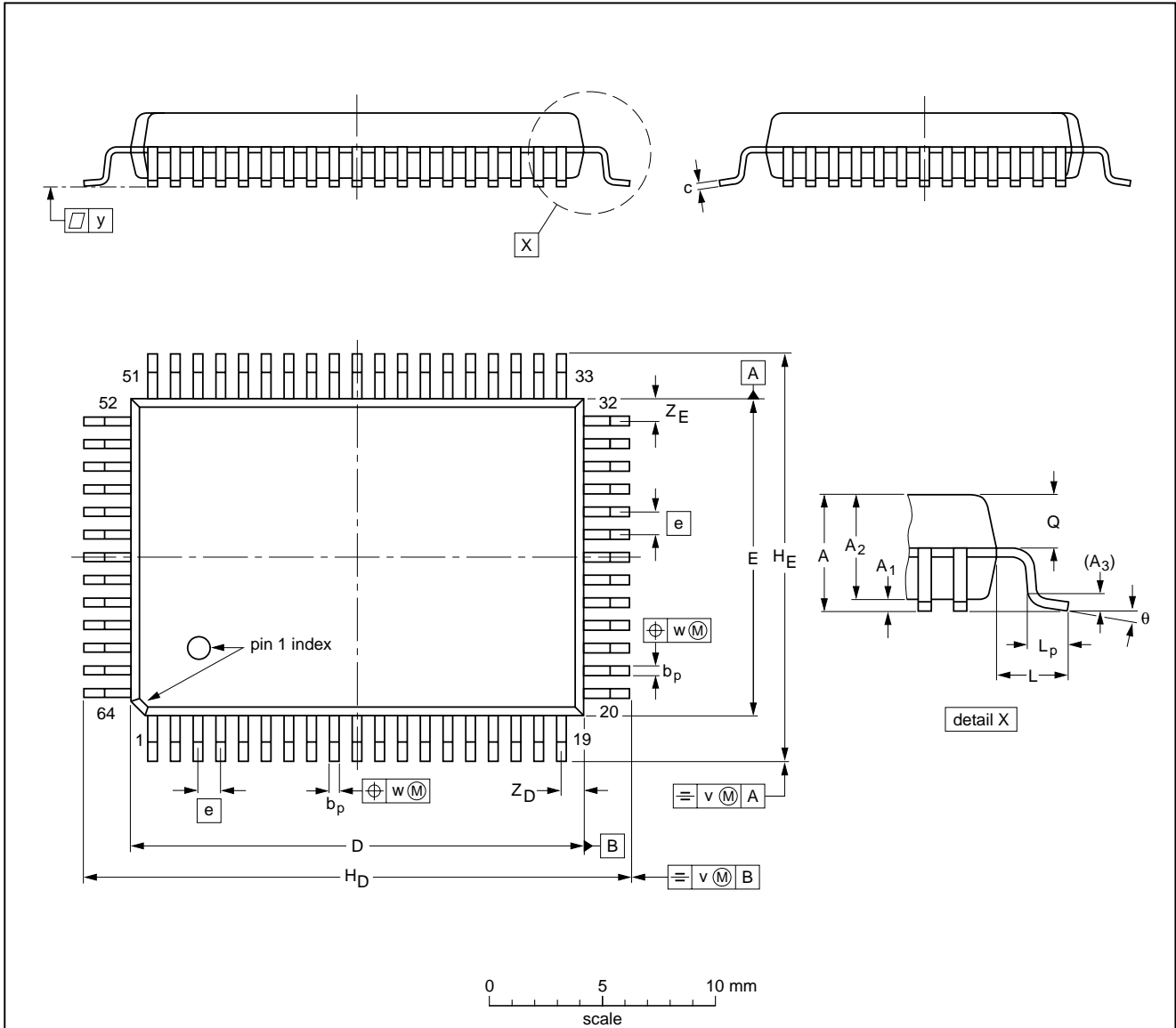
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PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT319-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	Q	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						92-11-17 95-02-04

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

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Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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